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1 impossible for the Applicant to fully address this issue. If the Examiner believes
2 that particular elements of claim 15 are missing from the drawings, it is requested
3 that such elements be identified. Otherwise, it is respectfully submitted that this
4 rejection of claim 15 is unfounded, and should be withdrawn.

5 6 **Title**

7 The title is objected to because the title is not descriptive. The title has
8 been amended to "Translating Data to Reduce Worst Case Power Consumption".

9 10 **Abstract**

11 The abstract of the disclosure is objected to because it is not clearly
12 indicative of the invention to which the claims are directed. A new abstract has
13 been provided.

14 15 **Typographical Corrections**

16 Two typographical errors have been corrected: on page 2 line 18 of the
17 specification, the equation " $P+fCV^2$ " should be $--P=fCV^2--$; on page 18 line 5, the
18 word "away" should be $--way--$.

19 20 **35 U.S.C. §112 Rejections**

21 Claim 39 is rejected as having "undue breadth" under §112. In supporting
22 this rejection, the Examiner cites the MPEP for the proposition that a single
23 "means" claim is improper. However, claim 39 is not a "means" claim, but a
24 *method* claim. The Examiner has shown no reason why a method claim
25 containing a single step is improper. Furthermore, the undersigned is not aware of

1 any authority for rejecting a method claim for the sole reason that it recites a
2 single step. Accordingly, the §112 rejection of claim 39 is not valid, and should
3 be withdrawn.

4 Claims 8-10, 12-15, 22, 24-25, 30, 33 and 41-43 have been rejected as
5 being indefinite. These rejections have been addressed by amendment except as
6 indicated below.

7 In several claims, the Office Action concludes that in recitations of the form
8 "... to receive first data ..." or "... to receive second data ..." (claims 8, 9, 12,
9 22, 25, 30, 33, 41 and 43), the term "first data" or "second data" does not have
10 antecedent basis. It is respectfully submitted that this conclusion is incorrect.
11 Grammatically, the term "data" is plural, and prefacing it with an "a" would be
12 grammatically incorrect: the phrase "a first data" or "a second data" would not be
13 grammatically correct. Rather, the first use of this term is properly phrased as "...
14 to receive first data" or "... to receive second data", while subsequent references
15 to "first data" are properly phrased as "the first data," and to "second data" are
16 properly phrased as "the second data." This issue arises in the §112 rejections of
17 claims 8, 9, 12, 22, 25, 30, 33, 41 and 43.

18 The remaining §112 issues are discussed on a claim-by-claim basis below.

19 In claim 8, reference to "the circuit" has been omitted. Antecedent basis
20 exists for "the first XOR circuit", on the second line of the claim. Similarly,
21 antecedent basis for "the first format" is found in the third line of the claim.

22 Claim 9 is now recites "a memory" rather than "the memory". Antecedent
23 basis for "the first data" is found in parent claim 8.

24 As to claim 10, antecedent basis for "the memory" is found in parent claim
25 8.

1 As to claim 12, antecedent basis for “the first data”, “the first format”, and
2 “the first XOR circuit” is provided in parent claim 8.

3 As to claim 13, antecedent basis for “the first format” is provided in parent
4 claim 8.

5 Amended claim 15 recites “a first plurality of XOR circuits” which
6 provides antecedent basis for the later recitation of “the first plurality of XOR
7 circuits” in claim 15.

8 As to claim 22, parent claim 15 recites “a first plurality of XOR circuits
9 each having a first input” which provides an antecedent basis for “the first inputs
10 of the first plurality of XOR circuits” in claim 22. Claim 22 has been amended to
11 recite “a first format” rather than “the first format”. Parent claim 15 recites “a first
12 plurality of XOR circuits each having ... an output” which provides an antecedent
13 basis for the “the outputs of the first plurality of XOR circuits.” Parent claim 18
14 recites “a second plurality of XOR circuits each having a first input ...and an
15 output”, which provides antecedent basis for “the first inputs of the second
16 plurality of XOR circuits” and for “the outputs of the second plurality of XOR
17 circuits.”

18 Claim 24 now recites “a memory” in the first line, rather than “the
19 memory”. Antecedent basis for “the first memory” is found in parent claim 22.

20 Claim 25 recites “a first plurality of XOR circuits”, which provides
21 antecedent basis for the later recitation of “the first plurality of XOR circuits.”

22 Amended claim 33 recites “a first plurality of XOR circuits” which
23 provides antecedent basis for the later recitation of “the first plurality of XOR
24 circuits” in claim 33.

1 Claim 41 has been amended to recite "the first data" rather than "the
2 reformatted data".

3 Claim 42 has been amended to recite "the first data" rather than "the
4 reformatted data".

5 Claim 43 has been amended to recite "the stored first data." Parent claim
6 41 recites and "storing" the first data, providing antecedent basis for "the stored
7 first data". Claim 41 also recites "a bus interface" providing an antecedent basis
8 for "the bus interface" in claim 43.

9
10 **35 U.S.C. §102 Rejections**

11 Claims 8-14 and 39-47 are rejected under 35 U.S.C § 102 as being
12 anticipated by U.S. Patent 4,397,022 by Weng et al. (Weng). In Figs. 1 and 2,
13 Weng discloses a parity generation circuit having XOR devices 125 (represented
14 in Fig. 1 by "+" symbols surrounded by circles). A data signal is routed serially
15 through XOR gate 125f and through a sequence of XOR gates 125a-125e, with
16 delay elements 110 between of the XOR gates 125a-125e. Specifically, the data
17 signal is routed from the output of 125f to a first input of 125a; from the output of
18 125a, through delay elements 110 to the first input of 125b; from the output of
19 125b, through further delay elements 110 to the first input of 125c; and so on
20 through 125d and 125e. In addition, the same data signal (as output from XOR
21 gate 125f) is connected in common to the second inputs of XOR gates 125a-125e.

22 Claim 8, as amended above, recites a first XOR circuit whose first input
23 receives first data and whose second input receives "a periodic signal *other than*
24 *the first data*". In addition, the second XOR circuit's second input also receives
25 "the periodic signal *other than the first data*". This is contrary to Weng, in which

1 a data signal is chained through the first inputs of XOR circuits 125a-125e, and the
2 same data signal is also connected to the second input of each XOR circuit.

3 In order to support a §102 rejection, a reference such as Weng must show
4 every element of a claim, in the exact manner claimed. In the case of claim 8,
5 Weng does not meet this requirement. Specifically, Weng does not show that the
6 second inputs of the XOR circuits receive a “periodic signal *other than the first*
7 *data.*” Accordingly, the rejection of claim 8 is not supported by the cited art, and
8 should be withdrawn.

9 Dependent claims 9-14 are allowable by virtue of their dependency on
10 respective base claim 8, as well as for the additional element recited therein which
11 are not disclosed by Weng in the claimed environment.

12 Claim 39 as amended above recites writing data to the memory device via a
13 first XOR circuit clocked by “a periodic signal *other than the data.*” This is
14 contrary to Weng, in which a data signal is chained through the first inputs of
15 XOR circuits 125a-125e, and the same data signal is also connected to the second
16 input of each XOR circuit. Accordingly, the rejection of claim 39 is not supported
17 by the cited art, and should be withdrawn.

18 Dependent claim 40 is allowable by virtue of its dependency on respective
19 base claim 39, as well as for the additional elements recited therein which are not
20 disclosed by Weng in the claimed environment.

21 Claim 41 recites “accessing a memory device” that includes “providing first
22 data” to the memory device in “a first format and at a first data rate.” The data is
23 reformatted to a second format in response to an *address signal*, where the second
24 format has a data rate different than the first data rate. The reformatted data is
25 stored in the memory device using the second format.

1 The Examiner has not attempted to show where an address signal is used in
2 Weng. In order to support a 102 rejection, the Examiner is obligated to point the
3 supposed correlation between recited elements and those same elements shown by
4 the prior art. The Examiner has failed to do this with regard to claim 41.
5 Accordingly, the rejection of claim 41 is not supported by the cited art, and should
6 be withdrawn.

7 Similarly, dependent claim 42 recites elements that are not addressed in the
8 Office Action. Specifically, claim 42 recites storing uncomplemented and
9 complemented data at even and odd addresses. The Office Action fails to
10 acknowledge these recited elements. Accordingly, it is respectfully requested that
11 the rejection of claim 42 be withdrawn.

12 Claim 43 is allowable by virtue of its dependency on base claim 41, as well
13 as for the additional elements recited therein which are not disclosed by Weng in
14 the claimed environment.

15 Independent claim 44 recites “. . . in response to an address signal on the
16 address bus . . .”. Again, the Office Action fails to address this recitation.
17 Accordingly, it is respectfully requested that the rejection of claim 44 be
18 withdrawn.

19 Claims 45-47 also recite the “address signal”, and are allowable in addition
20 for their dependent from allowable base claim 44.
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2 **Conclusion**

3 All pending claims are in condition for allowance. Applicants respectfully
4 request reconsideration and prompt issuance of the subject application. If any
5 issues remain that prevent issuance of this application, the Examiner is urged to
6 contact the undersigned attorney before issuing a subsequent Action.

7
8 Respectfully Submitted,

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10 Dated: 9/12/02

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1 **MARKED UP SPECIFICATION PARAGRAPHS AND CLAIMS**

2 **In the Specification**

3 The paragraph/equation at page 2, line 18, is amended as follows:

4
$$P [+]\equiv fCV^2$$

6 The paragraph at page 18, lines 3-7, is amended as follows:

7 For one embodiment, reformatting circuitry 106 is configured
8 like circuitry 55 from Figure 3 and supplies data from circuit 102 to
9 circuit 108. Reformatting circuitry 104 is configured in the opposite
10 [away] way, and supplies data from circuit 108 to circuit 102. Thus,
11 reformatting circuitry 104 is similar to circuitry 55, but supplies data
12 in the opposite direction.

13
14 **In the Claims**

15 Claims 8, 9, 15, 22, 24, 25, 33, 35, 39-43 are amended as follows:

16 8. **(Once Amended)** An apparatus comprising:

17 a first [exclusive-OR (XOR)] XOR circuit having a first input [coupled to
18 the circuit to provide the] to receive first data in a first format, a second input to
19 receive a periodic signal other than the first data; and an output to provide the first
20 data in a second format; and

21 a second XOR circuit having a first input coupled to the output of the first
22 XOR circuit, a second input coupled to receive the periodic signal other than the
23 first data, and an output to provide the first data in the first format.

1 **9. (Once Amended)** The apparatus of claim 8, further comprising a
2 memory for storing the first data in the second format.
3

4 **15. (Once Amended)** An apparatus comprising:
5 a first circuit having a plurality of terminals;
6 a first plurality of [exclusive-OR (XOR)] XOR circuits each having a first
7 input coupled to one of the plurality of terminals, a second input coupled to
8 receive a first periodic signal, and an output; and
9 a second circuit having a first plurality of terminals each coupled to an
10 output of one of the first plurality of XOR circuits, and a second plurality of
11 terminals, wherein a number of the first plurality of terminals is different than a
12 number of second plurality of terminals.
13

14 **22. (Once Amended)** The apparatus of claim 21, wherein the first
15 inputs of the first plurality of XOR [gates]circuits are each coupled to the first
16 circuit to receive first data in [the] a first format at a first data rate of the first
17 periodic signal, and the outputs of the first plurality of XOR [gates]circuits are
18 structured to provide the first data in a second format to the second circuit, and
19 wherein the first inputs of the second plurality of XOR [gates]circuits are each
20 coupled to the second circuit to receive the first data in the second format at a
21 second data rate of the second periodic signal, and the outputs of the second
22 plurality of XOR [gates]circuits are structured to output the first data in a third
23 format.
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1 **24. (Once Amended)** The apparatus of claim 22, wherein the first
2 circuit comprises a memory for storing the first data, and wherein the first periodic
3 signal comprises a first address signal for addressing the memory, and the second
4 periodic comprises a second address signal for addressing the memory.

5
6 **25. (Once Amended)** A system comprising:
7 a first device comprising:
8 a first circuit;
9 a first plurality of [exclusive-OR (XOR)] XOR circuits having first
10 inputs coupled to receive first data from the first circuit, second inputs each
11 coupled to receive a bit of a first predetermined number, and outputs; and
12 a second device comprising:
13 a second plurality of [exclusive-OR (XOR)] XOR circuits having
14 first inputs coupled to the outputs of the first plurality of XOR circuits, and second
15 inputs coupled to receive one bit of the first predetermined number.

16
17 **33. (Once Amended)** An apparatus comprising:
18 a first circuit;
19 a first plurality of [exclusive-OR (XOR)] XOR circuits having first inputs
20 coupled to receive first data from the first circuit, second inputs each coupled to
21 receive a bit of a predetermined number; and
22 a second circuit providing the first predetermined number to the first
23 plurality of XOR circuits.

1 **35. (Once Amended)** The apparatus of claim 33, wherein the
2 predetermined number is only one bit.

3
4 **39. (Once Amended)** A method of accessing a memory device
5 comprising:

6 writing data to the memory device via a first [exclusive-OR (XOR)] XOR
7 gate clocked by [the] a periodic signal other than the data.

8
9 **40. (Once Amended)** A method of accessing a memory device
10 comprising:

11 writing data to the memory device via first [exclusive-OR (XOR)] XOR
12 circuit clocked by a periodic signal other than the data; and

13 reading the data from the memory device via a second XOR circuit clocked
14 by the periodic signal.

15
16 **41. (Once Amended)** A method of accessing a memory device
17 comprising:

18 providing first data to a bus interface of the memory device in a first format
19 and at a first data rate;

20 reformatting the first data to a second format in response to an address
21 signal, the second format having a second data rate different than the first data
22 rate; and

23 storing the [reformatted] first data in the memory device in the second
24 format.

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1 **42. (Once Amended)** The method of claim 41, wherein the step of
2 storing the [reformatted] first data comprises storing uncomplemented first data at
3 even addresses, and storing complemented first data at odd addresses of the
4 memory device.

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6 **43. (Once Amended)** The method of claim 41, further comprising:
7 reformatting the stored first data into the first format; and
8 outputting the first data in the first format from the bus interface.
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